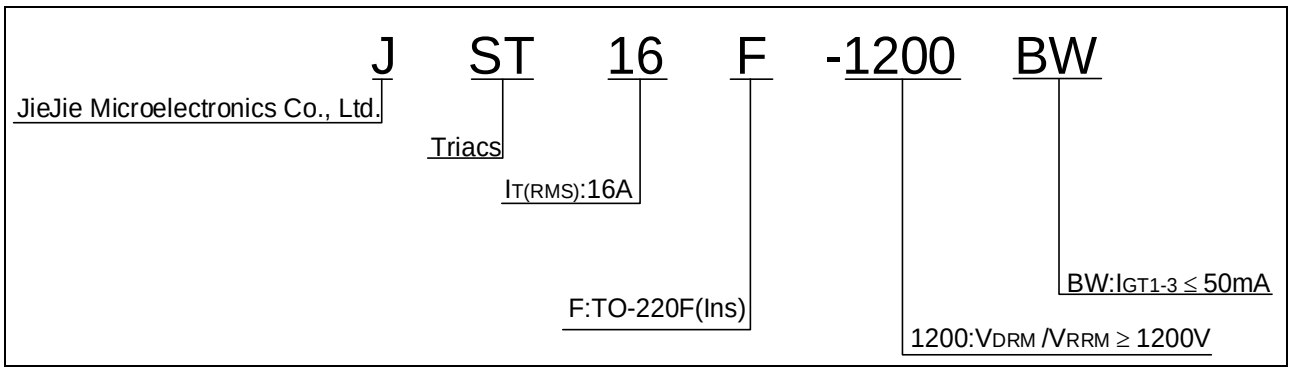
JST16]ˆ ~ ž ă яTRI ` C

Peak gate power	P_{GM}	10	W
Peak pulse voltage (T_j=25 ; non-repetitive,off-state;FIG.7)	V_{pp}	4	kV

(T_j=25 unless otherwise specified)

Symbol	Test Condition	Quadrant	Value		Unit
I_{GT}	V_D =12V R_L =33Ω	- -	MAX.	50	mA


J
ST
16
F
-1200
BW
JieJie Microelectronics Co., Ltd.
Triacs
IT(RMS):16A
F:TO-220F(Ins)
1200:VDRM /VRRM ≥ 1200V
BW:IGT1-3 ≤ 50mA

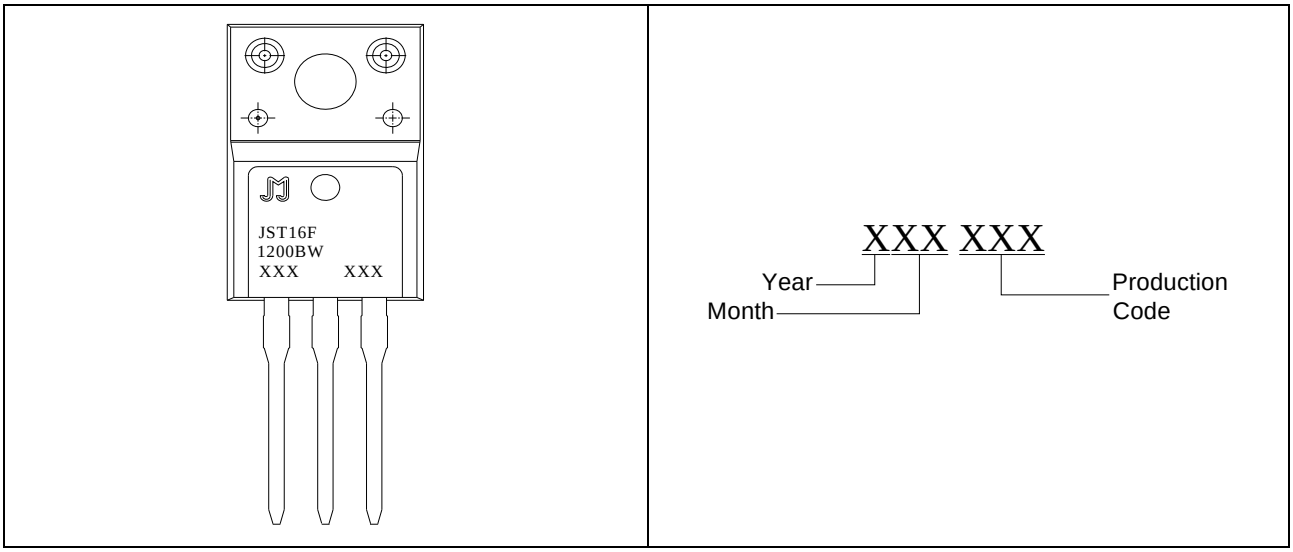

JST16F
1200BW
XXX XXX
XXX XXX
Year
Month
Production
Code

FIG.1: Maximum power dissipation versus RMS on-state current

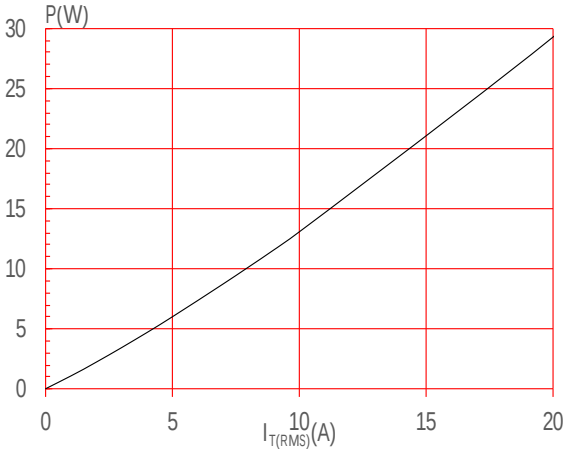


FIG.2: RMS on-state current versus case temperature

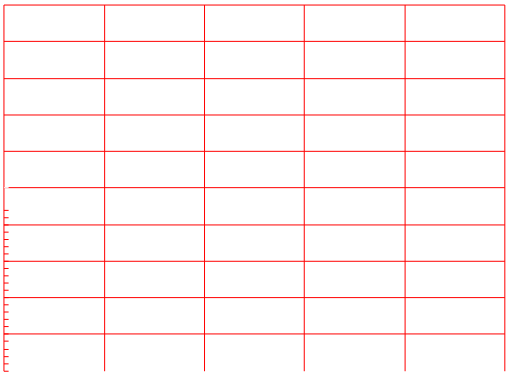


FIG.7 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards

Order code	Voltage V_{DRM}/V_{RRM} (V)	IGT(mA)	Package	Base qty. (pcs)	Delivery mode
		-			

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